

General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.
- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.
- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.
- This document is paginated as submitted by the original source.
- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

(NASA-CR-161131) DIODE STEP STRESS PROGRAM
FOR JANTX1N5415 Final Report (DCA
Reliability Lab., Sunnyvale, Calif.) 39 p
HC A03/MF A01 CSCI 09A

N79-18210

Unclas
14165
G3/33

DIODE STEP STRESS TESTING PROGRAM

MSFC/NASA CONTRACT NUMBER
NAS8-31944

FINAL REPORT
FOR
JANTX 1N5415

JANUARY 1979

Prepared
For

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Marshall Space Flight Center, Alabama 35812

DCA RELIABILITY LABORATORY
SPECIAL PRODUCTS DIVISION
975 BENICIA AVE
SUNNYVALE, CALIFORNIA 94086





FOREWORD

This report is a summary of the work performed on NASA Contract NAS8-31944. The investigation was conducted for the National Aeronautics and Space Administration, George C. Marshall Space Flight Center, Huntsville, Alabama. The Contracting Officer's Technical Representative was Mr. F. Villella.

The short-term objective of this preliminary study of transistors, diodes, and FETS is to evaluate the reliability of these discrete devices, from different manufacturers, when subjected to power and temperature step stress tests.

The long-term objective is to gain more knowledge of accelerated stress testing for use in future testing of discrete devices, as well as to determine which type of stress should be applied to a particular device or design.

This report is divided as follows: description of tests, figures, tables, and appendix.

**TABLE OF CONTENTS**

	<u>Page</u>
1.0 INTRODUCTION	1
2.0 TEST REQUIREMENTS	1
2.1 Electrical	1
2.2 Stress Circuit	1
2.3 Group I - Power Stress	2
2.4 Group II - Temperature Stress I	2
2.5 Group III - Temperature Stress II	2
3.0 DISCUSSION OF TEST RESULTS	3
3.1 Group I - Power Stress	3
3.1.1 Semtech	3
3.1.2 Micro Semiconductor	4
3.1.3 Statistical Summary - Group I	4
3.2 Group II - Temperature Stress I	5
3.2.1 Semtech	5
3.2.2 Micro Semiconductor	5
3.2.3 Statistical Summary - Group II	6
3.3 Group III - Temperature Stress II	6
3.3.1 Semtech	6
3.3.2 Micro Semiconductor	6
3.3.3 Statistical Summary - Group III	7
4.0 FINAL DATA SUMMARY	7
5.0 CONCLUSIONS	8

**LIST OF ILLUSTRATIONS**

<u>Figure</u>	<u>Title</u>	<u>Page</u>
1	Power and Temperature Stress Circuit for JANTX1N5415	11
2	Cumulative Percent Failures Versus Junction Temperature, Semtech	12
3	Time Steps Versus Junction Temperature, Semtech	13 .
4	Cumulative Percent Failures Versus Junction Temperature, Micro Semiconductor	14
5	Time Steps Versus Junction Temperature, Micro Semiconductor	15
A-1	S/N 7366. Magnification 10X	30
A-2	S/N 7392. Magnification 10X	30
A-3	S/N 7419. Magnification 10X	31
B-1	S/N 7397. Magnification 10X	34

**LIST OF TABLES**

<u>Table</u>	<u>Title</u>	<u>Page</u>
1	Test Flow Diagram	16
2	Parameters and Test Conditions	17
3	Power Stress Burn-In Conditions	17
4	Group I - Power Stress Data Summary	19
5	Group II - Temperature Stress I Data Summary	21
6	Group III - Temperature Stress II Data Summary	22
7	Final Data Summary	23
8	Step Stress Catastrophic Failure Summary	24
9	Step Stress Parametric Failure Summary	25



1.0 INTRODUCTION

DCA Reliability Laboratory, under Contract NAS8-31944 for NASA/Marshall Space Flight Center, has compiled data for the purpose of evaluating the effect of power/temperature step stress when applied to a variety of semiconductor devices. This report covers the diode JANTX1N5415 manufactured by SEMTECH and MICRO SEMICONDUCTOR.

A total of 48 samples from each manufacturer were submitted to the process outlined in Table 1. In addition, two control sample units were maintained for verification of the electrical parametric testing.

2.0 TEST REQUIREMENTS

2.1 Electrical

All test samples were subjected to the electrical tests outlined in Table 2 after completing the prior power/temperature step stress point. These tests were performed using the Fairchild Model 600 High-Speed Computer-Controlled Tester. Additional bench testing was also required on the devices.

2.2 Stress Circuit

The test circuit shown in Figure 1 was used to power all the test devices during the power/temperature stress conditions. The voltage was set by V_F and the current was varied in order to comply with the specified power rating for the device. At least one of the devices was subjected to maximum rated power (MRP). All remaining devices were



subjected to no less than 90% of MRP. See Figure 1 for load resistance values and voltages.

2.3 Group I - Power Stress

Thirty-two units, 16 from each manufacturer, were submitted to the Power Stress Process. The diodes were stressed in 500-hour steps at 50, 100, 125, 150 and 175 percent of maximum rated power (MRP) for 2500 hours or until 50% or more of the devices in a sample lot failed.* Electrical measurements were performed on all specified electrical parameters after each power step. See Table 1. (*See Notes at end of text.)

2.4 Group II - Temperature Stress I

Thirty-two units, 16 from each manufacturer, were submitted to the Temperature Stress I Process. Group II was subjected to 1600 hours of stress at maximum rated power in increments of 160 hours. The temperature was increased in steps of 25°C, commencing at 75°C and terminating at 300°C or until 50% or more of the devices failed.* Electrical measurements were performed on all specified electrical parameters after each temperature step. See Table 1.

2.5 Group III - Temperature Stress II

Thirty-two units, 16 from each manufacturer, were submitted to the Temperature Stress II Process. Group III was subjected to 112 hours of stress at maximum rated power in increments of 16 hours. The temperature was increased in steps of 25°C, commencing at 150°C and terminating at 300°C or until 50% or more of the devices in a sample lot



failed.* Electrical measurements were performed on all specified electrical parameters after each temperature step. See Table 1.

3.0 DISCUSSION OF TEST RESULTS

3.1 Group I - Power Stress

3.1.1 Semtech. The Semtech sample lot completed 550 hours of Group I Testing at which point 50% of the lot failed. The lot continued processing an additional 700 hours and had three more failures. The first failures occurred 150 hours into the 50% MRP step. Serial numbers 7387, 7388, 7389, 7391 and 7392 failed due to excessive I_R leakage. The next failures occurred 250 hours into the 50% MRP step. Serial numbers 7390 and 7393 failed due to excessive I_R leakage. Serial numbers 7388 and 7389 had remained in the testing and became visual rejects. (See Note B, Table 8). The next failure occurred 50 hours into the 100% MRP step. Serial number 7363 was a visual catastrophic reject. The next failure occurred 500 hours into the 100% MRP step. Serial number 7362 failed due to excessive I_R leakage. The next failures occurred 250 hours into the 125% MRP step. Serial numbers 7366 and 7367 were visual rejects. (See Note B, Table 8.) Typical characteristics of this lot's performance were:

- 1) The mean value for I_R changed 349.8nA from an initial mean of 33.40nA to a final mean of 382.2nA.
- 2) The mean value for V_{F1} changed 17.00mV from an initial mean of 1.268V to



a final mean of 1.285V.

- 3) The mean value for V_{F2} changed 4.100mV from an initial mean of 928.2mV to a final mean of 932.3mV.

The control units for this sample lot remained constant throughout the entire Group I Testing.

3.1.2 Micro Semiconductor. The Micro Semiconductor sample lot completed the entire 2500-hours of Group I Testing with four catastrophic failures. The first failures occurred 500 hours into the 150% MRP step. Serial numbers 7419, 7420 and 7421 were visual rejects. (See Note B, Table 8). The last failure occurred 25 hours into the 175% MRP step. Serial number 7425 failed due to excessive I_R leakage. Typical characteristics of this lot's performance were:

- 1) The mean value for I_R changed 90.60nA from an initial mean of 466.6nA to a final mean of 376.0nA.
- 2) The mean value for V_{F1} changed 10.10mV from an initial value of 921.5mV to a final mean of 911.4mV.
- 3) The mean value for V_{F2} changed 2.700mV from an initial mean of 764.8mV to a final mean of 762.1mV.

The control units for this sample lot remained constant throughout the entire Group I Testing.

3.1.3 Statistical Summary - Group I. Table 4 outlines the results of Group I - Power Stress Process for each of the three electrical parameters and all measurement points for both Semtech and Micro Semiconductor.



3.2 Group II - Temperature Stress I

3.2.1 Semtech. The Semtech sample lot completed 160 hours of the Group II Testing before the lot was stopped because of a 50% failure rate. The failures occurred 160 hours into the 75°C-temperature step. Serial numbers 7395, 7396, 7397, 7398, 7399, 7400, 7401 and 7402 failed due to excessive I_R leakage. Typical characteristics of this lot's performance were:

- 1) The mean value for I_R changed 2.712mA from an initial mean of 24.14nA to a final mean of 2.171mA.
- 2) The mean value for V_{F1} changed 300.0μV from an initial mean of 917.1mV to a final mean of 916.8mV.

The control units for this sample lot remained constant throughout the entire Group II Testing.

3.2.2 Micro Semiconductor. The MSC sample lot completed the entire 1600 hours of Group II Testing with no catastrophic failures. Typical characteristics of this lot's performance were:

- 1)) The mean value for I_R changed 3.926μA from an initial mean of 280.7nA to a final mean of 4.207μA.
- 2) The mean value for V_{F1} changed 2.400mV from an initial mean of 906.2mV to a final mean of 908.6mV.
- 3) The mean value for V_{F2} changed 4.700mV from an initial mean of 767.9mV to a final mean of 763.2mV.

The control units for this sample lot remained constant throughout the entire Group II Testing.



3.2.3 Statistical Summary - Group II. Table 5 of this report outlines the results of Group II - Temperature Stress I for each of the three electrical parameters and all of the measurement points pertaining to both Semtech and Micro Semiconductor.

3.3 Group III - Temperature Stress II

3.3.1 Semtech. The Semtech sample lot completed the entire 112 hours of Group II Testing with seven catastrophic failures. The first failures occurred 16 hours into the 150°C-temperature step. Serial numbers 7404, 7405, 7406, 7407, 7409 and 7410 failed due to excessive I_R leakage. The next failure occurred 16 hours into the 175°C-temperature step. Serial number 7408 failed due to excessive I_R leakage. Serial number 7376 was reported missing 16 hours into the 200°C-temperature step. Typical characteristics of this sample lot's performance were:

- 1) The mean value for I_R changed 165.8nA from an initial value of 19.52nA to a final mean of 185.3nA.
- 2) The mean value for V_{F1} changed 12.00mV from an initial mean of 1.276V to a final mean of 1.264V.
- 3) The mean value of V_{F2} changed 7.200mV from an initial value of 938.1mV to a final value of 930.9mV.

The control units for this sample lot remained constant throughout the entire Group III Testing.

3.3.2 Micro Semiconductor. The MSC sample lot completed



the entire 112 hours of Group III Testing with no catastrophic failures. Typical examples of this lot's performance were:

- 1) The mean value for I_R changed 44.20nA from an initial mean of 279.6nA to a final mean of 323.8nA.
- 2) The mean value for V_{F1} changed 3.800mV from an initial mean of 936.1mV to a final mean of 939.9mV.
- 3) The mean value for V_{F2} changed 2.700mV from an initial mean of 781.0mV to a final mean of 778.3mV.

The control units for this sample lot remained constant throughout the entire Group III Testing.

3.3.3 Statistical Summary - Group III. Table 6 outlines the results of Group III - Temperature Stress II Testing, for each of the electrical parameters and all of the measurement points for both Semtech and Micro Semiconductor.

4.0 FINAL DATA SUMMARY

Table 7 statistically summarizes the change in the mean value from the zero-hour data to the final data. The graphs of Figures 2 and 4 plot the cumulative percent failures versus the temperature stress level for Group II - Temperature Stress I, and Group III - Temperature Stress II. The graphs of Figures 3 and 5 plot the time step for Group II (160 hours) and Group III (16 hours) versus the temperatures T_1 and T_2 calculated from Figures 2 and 4. Tables 8 and 9 summarize the failures encountered for all three stress groups. The failures are separated into two categories:



catastrophic failures in Table 8 and parametric failures in Table 9. The data from Table 8 were used as a source for the graphs in Figures 2 and 4. Figures 2 and 4 were used as a source for the graphs in 3 and 5, respectively. Junction temperature is plotted on an inverse hyperbolic scale.

5.0 CONCLUSIONS

While the Semtech sample lots suffered large failure rates in all three stress tests, the Micro Semiconductor sample lots experienced no failures in the Group II and III Testing and only four in the Group I Testing.

There were two types of failures throughout all three stress tests for both manufacturers. One was a visual catastrophic reject. The failures were still within the electrical limits of the test when they became visual failures due to a loss of an external lead.

The second type of failure was the reverse bias leakage. The main cause of this failure was the conductive external paint on the diodes. When the continuity of the paint was interrupted by means of sandpaper, the reverse leakage fell to acceptable levels.

A complete plot showing cumulative failure distribution and activation energy for Semtech could not be extrapolated due to an early excessive failure rate in the Group II Testing (Figures 2 and 3). A plot for the Micro Semiconductor lot could not be plotted due to an absence of failure points in the Groups II and III Testing (Figures 4 and 5).



A broken circle around a marked point on the graph indicates a freak failure not calculated as part of the regression line. A solid circle around a marked point indicates an isolated main failure point. The regression line was calculated using the least squares method.

The activation energy was calculated from the formula:

$$E = \left[\ln \left(\frac{t_1}{t_2} \right) \right] \left[\frac{8.63 \times 10^{-5} \text{ eV/}^\circ\text{K}}{\left(\frac{1}{T_1 + 273} \right) - \left(\frac{1}{T_2 + 273} \right)} \right] \text{ eV}$$

Where: t_1 = step of Group II - Temp Stress I = 160 hrs.

t_2 = step of Group III - Temp Stress II = 16 hrs.

T_1 = temperature in $^\circ\text{C}$ of 16% failure for Group II.

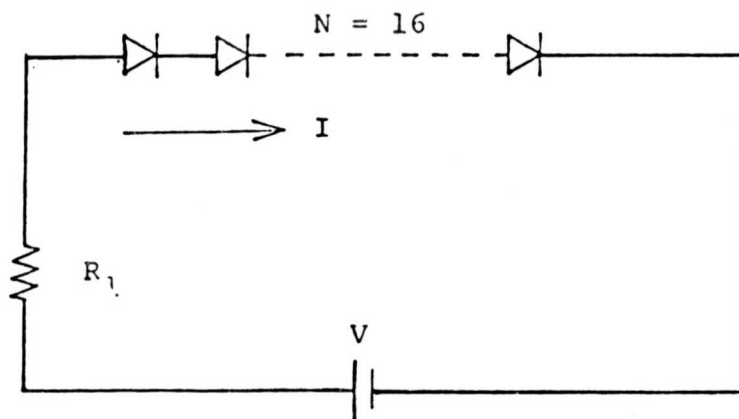
T_2 = temperature in $^\circ\text{C}$ of 16% failure for Group III.



NOTE:

* Conditions for failure:

- A) Open or short
- B) Leakage exceeds the maximum limit by 100 times
- C) Other parameters exceed MIL limits by 50% or more.

SWITCHING DIODES

$$R_1 = 1V/I \pm 1\%$$

$$P_d = IE$$

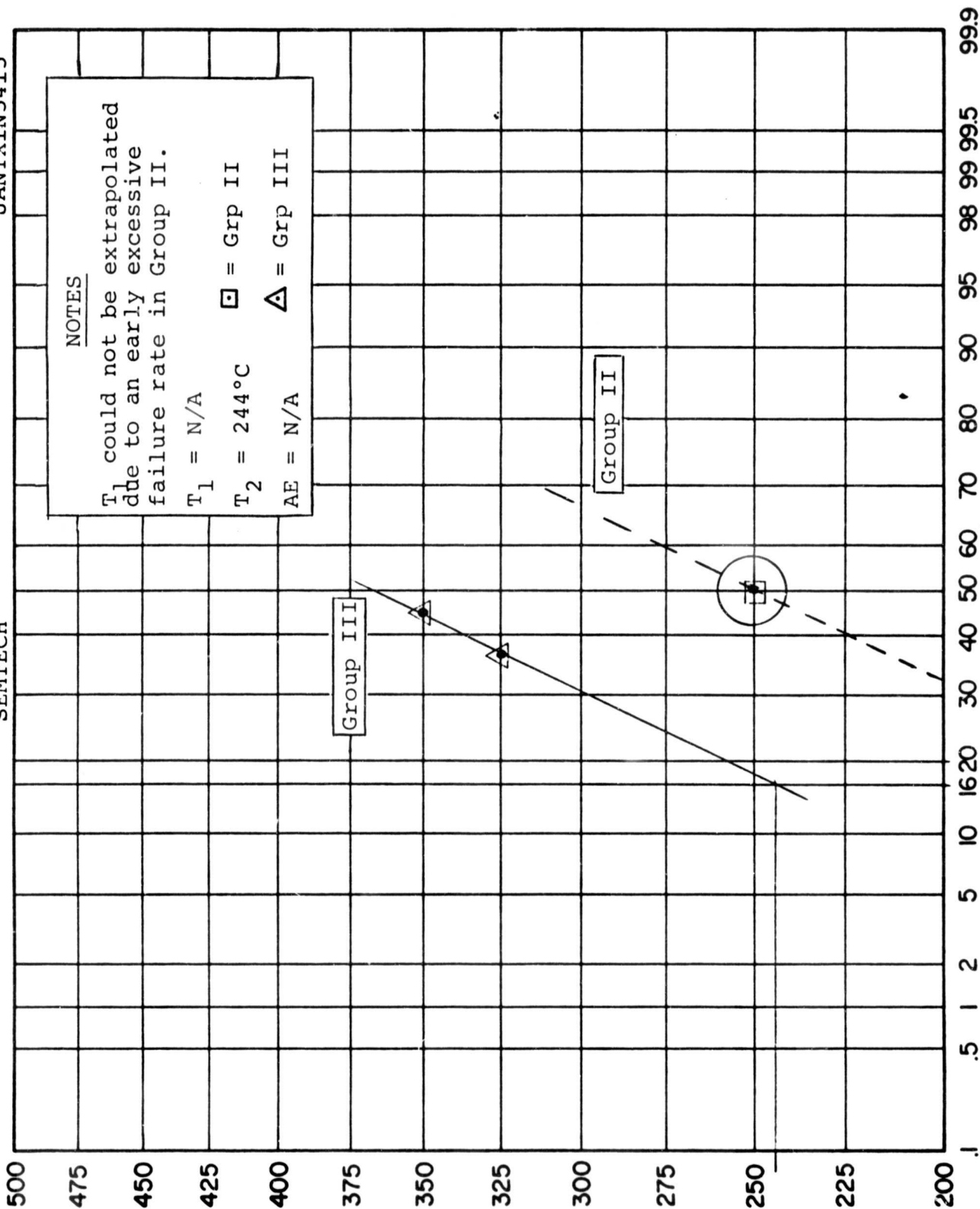
FIGURE 1
Power/Temperature Stress Circuit
for JANTX1N5415



SEMTECH

JANTX1N5415

JANTX1N5415



NOTES

T₁ could not be extrapolated due to an early excessive failure rate in Group II.

T₁ = N/A

T₂ = 244°C

AE = N/A

□ = Grp II

△ = Grp III

*NOTE

T_J ≈ T_A + 175°C

FIGURE 2
Cumulative Percent Failures Versus Junction Temperature, Semtech

SEMTECH

SE...

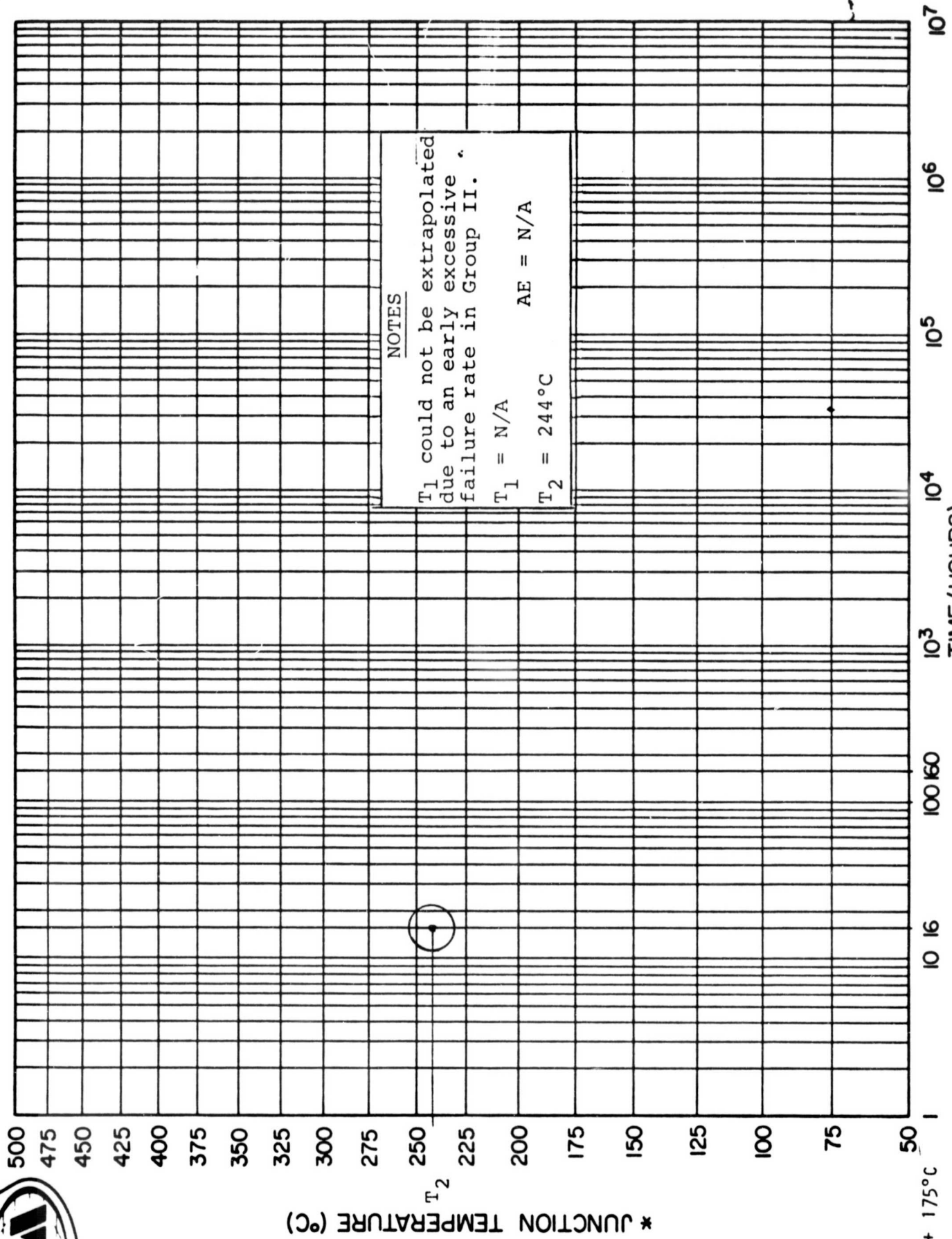


FIGURE 3
Time Steps Versus Junction Temperature, Semtech



MICRO SEMICONDUCTOR

JANTX1N5415

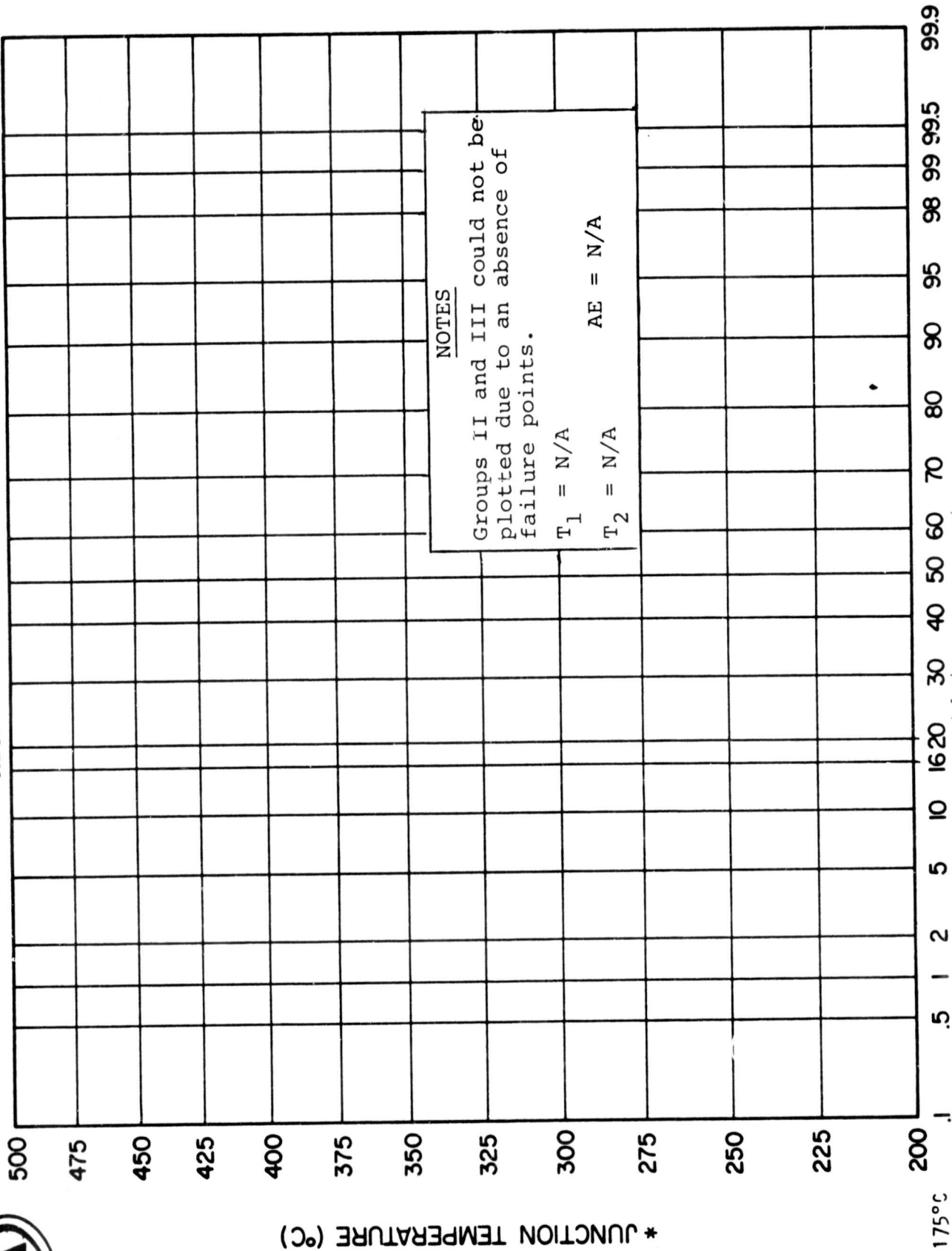
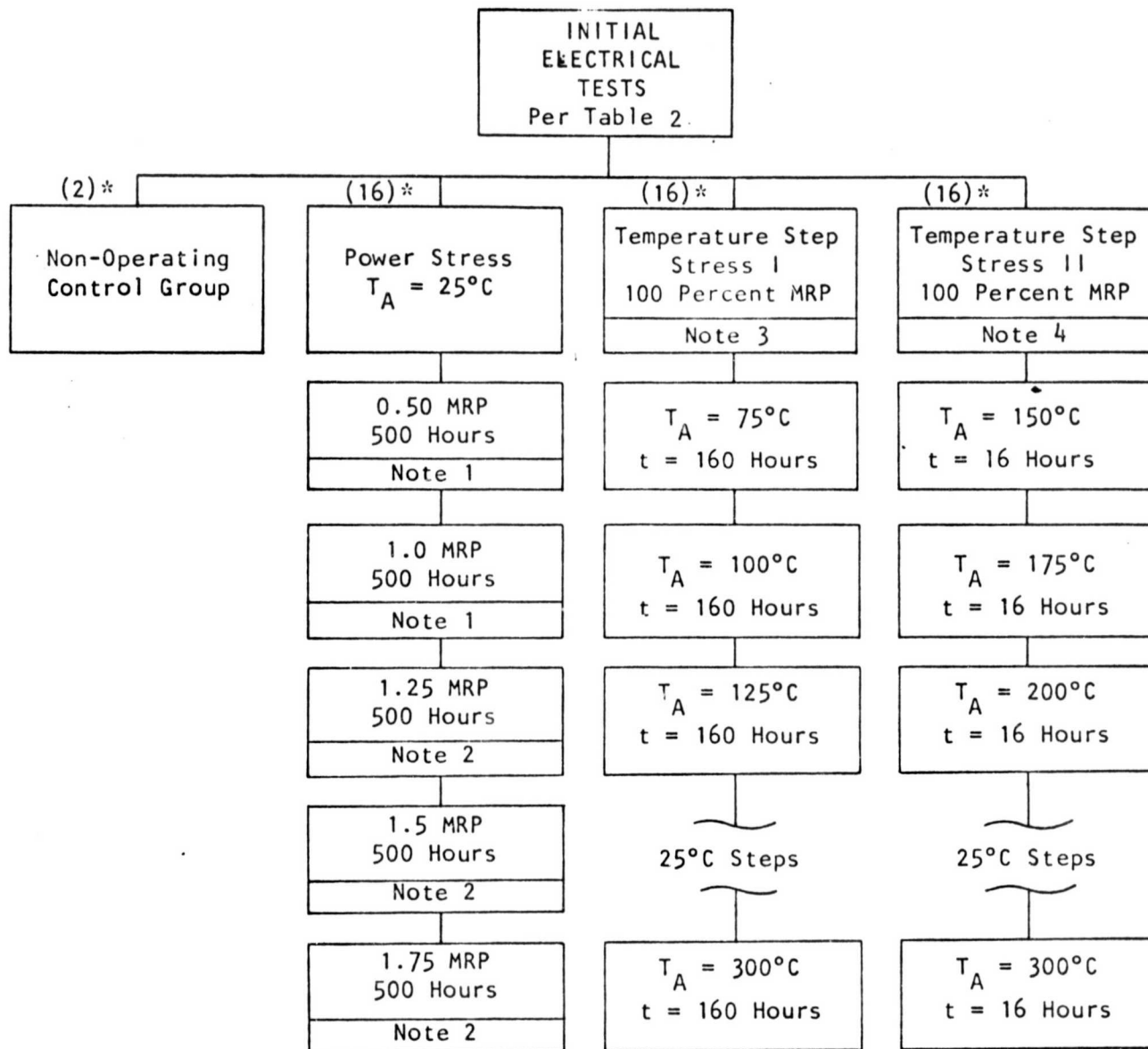


FIGURE 4
Cumulative Percent Failures Versus Junction Temperature, MSI


$$T_J \approx T_A + 175^\circ\text{C}$$

FIGURE 5
Time Steps Versus Junction Temperature, MSI

TABLE 1
TEST FLOW DIAGRAM

*Quantity per manufacturer (Semtech and Micro Semiconductor)

NOTES:

- 1) Electrical measurements per Table 2 were made at 50, 150, 250 and 500 hours.
- 2) Electrical measurements per Table 2 were made at 10, 25, 50, 150, 250 and 500 hours.
- 3) Electrical measurements per Table 2 were made at the end of each 160 hours.
- 4) Electrical measurements per Table 2 were made at the end of each 16 hours.



TABLE 2
PARAMETERS AND TEST CONDITIONS

PARAMETER	CONDITIONS	SPEC. LIMIT		CAT. LIMIT		UNITS
		MIN	MAX	MIN	MAX	
I_R	$V_R = 50V$	-	1.0	-	100.0	μA
V_{F1}	$I_F = 9A$ (Pulsed)	.6	1.5	.3	2.25	V
V_{F2}	$I_O = 2A$ (Not Pulsed)	.6	1.2	.3	1.8	V

NOTES:

1/ In addition, any open or short shall be considered catastrophic

TABLE 3
POWER STRESS BURN-IN CONDITIONS

$V_F =$	
$I_F =$	Percent P_D
1.8A	50
3.6A	100
4.5A	125
5.4A	150
6.3A	175



NOTE
FOR TABLES
4 THROUGH 7

The minimum/maximum initial and final data generally have an absolute accuracy of $\pm 1\%$ of the reading and $\pm$ one digit except for readings greater than 9.99mA which have an absolute accuracy of $\pm 2\%$ of the reading and $\pm$ one digit. The data also have a resolution for four digits. The standard deviations, means, delta means, and average means are, therefore, valid indicators of trends over time and temperature, excepting the minor statistical computer error of supplying a constant number of significant digits.



TABLE 4

GROUP I - POWER STRESS DATA SUMMARY

Page 1 of 2

PARAMETER	$I_R = 1\mu A(\text{MAX})$	$V_{F1} = .6V(\text{MIN})$	$1.5V(\text{MAX})$	$V_{F2} = .6V(\text{MIN})$	$1.2V(\text{MAX})$
CONDITIONS AND LIMIT	$V_R = 50V$	$I_F = 9A$ (Pulsed)		$I_O = 2A$ (Not Pulsed)	
IDENTIFICATION	SEM	MSC	SEM	MSC	SEM
INITIAL DATA					
MIN VALUE	18.30nA	203.0nA	1.110V	896.0mV	879.8mV
MAX VALUE	59.60nA	894.0nA	1.410V	963.0mV	981.8mV
MEAN	33.40nA	466.6nA	1.268V	921.5mV	928.2mV
STD DEV	14.39nA	249.1nA	99.09mV	16.99mV	912.7mV
INTERIM DATA					
POWER 50 TO 125% Δ MEAN VALUE					
50% POWER					
50 HRS	7.290nA	-74.30nA	0.000V	-3.800mV	0.300mV
150 HRS	*72.52 μA	-167.5nA	11.00mV	-7.600mV	-3.400mV
250 HRS	*807.7 μA	-220.7nA	17.00mV	-7.000mV	-0.100mV
500 HRS	3.024 μA	-79.00nA	73.00mV	-11.10mV	16.10mV
100% POWER					
550 HRS	190.8nA	-146.3nA	87.00mV	-9.700mV	29.60mV
650 HRS	5.195 μA	-135.9nA	66.00mV	-10.80mV	10.50mV
750 HRS	11.95 μA	-169.8nA	99.00mV	-8.400mV	33.90mV
1000 HRS	*63.38 μA	-223.8nA	92.00mV	-25.20mV	18.90mV
125% POWER					
1010 HRS	1.741 μA	-191.0nA	99.00mV	-6.500mV	32.00mV
1025 HRS	6.961 μA	-163.6nA	99.00mV	-5.700mV	33.50mV
1050 HRS	258.6nA	-130.2nA	47.00mV	-7.200mV	10.00mV
1150 HRS	215.1nA	-218.2nA	44.00mV	-23.20mV	6.10mV
1250 HRS	349.8nA	-221.3nA	17.00mV	-1.500mV	4.100mV
1500 HRS	JOB STOPPED	-196.0nA	JOB STOPPED	-28.60mV	JOB STOPPED

(continued on second sheet)

TABLE 4 (Cont'd)
— POWER STRESS DATA SUMMARY

Page 2 of 2

(continued from first sheet)

PARAMETER	GROUP I		GROUP II		GROUP III		GROUP IV		GROUP V		GROUP VI	
	$I_R = 1\mu A$ (MAX)	$V_F = 6V$ (MIN)	$I_F = 9A$ (Pulsed)	$V_F = 6V$ (MIN)	$I_F = 2A$ (Not Pulsed)	$V_F = 6V$ (MIN)	$I_F = 2A$ (Not Pulsed)	$V_F = 6V$ (MIN)	$I_F = 2A$ (Not Pulsed)	$V_F = 6V$ (MIN)	$I_F = 2A$ (Not Pulsed)	$V_F = 6V$ (MIN)
CONDITIONS AND LIMITS	$V_R = 50V$	$I_F = 9A$ (Pulsed)	$V_F = 6V$ (MIN)	$I_F = 2A$ (Not Pulsed)	$V_F = 6V$ (MIN)	$I_F = 2A$ (Not Pulsed)	$V_F = 6V$ (MIN)	$I_F = 2A$ (Not Pulsed)	$V_F = 6V$ (MIN)	$I_F = 2A$ (Not Pulsed)	$V_F = 6V$ (MIN)	$I_F = 2A$ (Not Pulsed)
IDENTIFICATION	SEM	MSC	SEM	MSC	SEM	MSC	SEM	MSC	SEM	MSC	SEM	MSC
INITIAL DATA												
MIN VALUE	18.30nA	203.0nA	1.110V	896.0mV	879.8mV	756.4mV						
MAX VALUE	59.60nA	894.0nA	1.410V	963.0mV	981.8mV	774.3mV						
MEAN	33.40nA	466.6nA	1.268V	921.5mV	928.2mV	764.8mV						
STD DEV	14.39nA	249.1nA	99.09mV	16.99mV	912.7mV	4.976mV						
INTERIM DATA												
POWER 150 TO 175% Δ MEAN VALUE												
150% POWER												
1510 HRS	JOB STOPPED	-199.1nA	JOB STOPPED	-2.900mV	JOB STOPPED	6.300mV						
1525 HRS		-135.2nA		-5.600mV		2.600mV						
1550 HRS		-140.4nA		-7.500mV		1.700mV						
1650 HRS		-182.2nA		-15.20mV		-7.500mV						
1750 HRS		-99.00nA		-5.600mV		4.800mV						
2000 HRS		-162.1nA		-6.700mV		4.700mV						
175% POWER												
2010 HRS		-129.4nA		-8.900mV		1.100mV						
2025 HRS		*92.90 μA		-8.500mV		1.700mV						
2050 HRS		-221.1nA		-5.100mV		7.100mV						
2150 HRS		-147.4nA		-8.600mV		2.100mV						
2250 HRS		-181.2nA		-7.500mV		3.600mV						
2500 HRS		-90.60nA		-10.10mV		-2.700mV						
FINAL DATA												
MIN VALUE	19.40nA	252.0nA	1.200V	886.0mV	898.0mV	751.0mV						
MAX VALUE	920.0nA	727.0nA	1.430V	957.0mV	984.0mV	771.0mV						
MEAN	382.2nA	376.0nA	1.285V	911.4mV	932.3mV	762.1mV						
STD DEV	383.3nA	120.4nA	901.4mV	17.30mV	31.88mV	6.512mV						

* NOTE: Catastrophic reject(s) removed from data after this point.

TABLE 5
GROUP II TEMP STRESS I DATA SUMMARY

PARAMETERS	$I_R = 1\mu A(\text{MAX})$		$V_{F1} = .6V(\text{MIN})$	$1.5V(\text{MAX})$	$V_{F2} = .6V(\text{MIN})$	$1.2V(\text{MAX})$
CONDITIONS AND LIMITS	$V_R = 50V$		$I_F = 9A \text{ (Pulsed)}$		$I_O = 2A \text{ (Not Pulsed)}$	
IDENTIFICATION	SEM	MSC	SEM	MSC	SEM	MSC
INITIAL DATA						
MIN VALUE	16.60nA	193.0nA	1.150V	891.0mV	851.0mV	760.0mV
MAX VALUE	53.80nA	613.0nA	1.410V	930.0mV	980.0mV	778.0mV
MEAN	24.14nA	280.7nA	1.261V	906.2mV	917.1mV	767.9mV
STD DEV	8.580nA	95.68nA	80.85mV	9.241mV	41.90mV	5.395mV
INTERIM DATA (INITIAL TO FINAL)						
Δ MEAN VALUE						
TOTAL HRS						
TEMP (T_A)						
75°C	*2.712mA	-17.70nA	6.000mV	5.300mV	-300.0mV	-0.100V
100°C	JOB STOPPED	22.70nA	JOB STOPPED	3.600mV	JOB STOPPED	-2.400mV
125°C		-33.60nA		6.200mV		1.200mV
150°C		-59.90nA		8.200mV		3.900mV
175°C		-19.00nA		4.400mV		-0.100mV
200°C		14.80nA		1.100mV		-5.500mV
225°C		58.70nA		1.400mV		-4.700mV
250°C		13.30rA		4.600mV		-0.600mV
275°C		663.10nA		0.300mV		-7.800mV
300°C		3.926 μA		2.400mV		-4.700mV
FINAL DATA						
FINAL TEMP (T_A)						
75°C						
300°C						
MIN VALUE	18.50nA	351.0nA	1.140V	894.0mV	851.0mV	754.0mV
MAX VALUE	7.630mA	12.20 μA	1.420V	932.0mV	980.0mV	773.0mV
MEAN	2.712mA	4.207 μA	1.267V	908.6mV	916.8mV	763.2mV
STD DEV	2.972mA	3.593 μA	84.17mV	9.157mV	41.27mV	5.187mV

* NOTE: Catastrophic reject(s) removed from data after this point.

TABLE 6
GROUP III TEMP STRESS II DATA SUMMARY

PARAMETERS	$I_R = 1\mu A (MAX)$		$V_{F1} = .6V (MIN)$	$1.5V (MAX)$	$V_{F2} = .6r (MIN)$		$1.2V (MAX)$
CONDITIONS AND LIMITS	$V_R = 50V$		$I_F = 9A (Pulsed)$		$I_O = 2A (Not Pulsed)$		
IDENTIFICATION	SEM	MSC	SEM	MSC	SEM	MSC	
INITIAL DATA							
MIN VALUE	12.50nA	209.0nA	1.170V	911.0mV	878.0mV	770.0mV	
MAX VALUE	37.70nA	414.0nA	1.380V	972.0mV	999.0mV	791.0mV	
MEAN	19.52nA	279.6nA	1.276V	936.1mV	938.1mV	781.0mV	
STD DEV	5.528nA	60.93nA	74.66mV	16.65mV	40.38mV	5.534mV	
INTERIM DATA (INITIAL TO FINAL)							
Δ MEAN VALUE							
TOTAL HRS							
TEMP (T_A)							
16	*278.2 μA	123.3nA	34.00mV	-4.000mV	-6.300mV	-9.900mV	
32	*505.5 μA	58.80nA	27.00mV	-7.800mV	-6.900mV	-4.900mV	
48	22.89nA	83.30nA	21.00mV	-11.30mV	-10.80mV	-10.40mV	
64	238.4nA	173.3nA	27.00mV	-8.800mV	-19.40mV	-6.100mV	
80	100.7nA	148.1nA	-12.00mV	-10.00mV	-10.60mV	-7.700mV	
96	117.8nA	75.60nA	24.00mV	-4.900mV	-10.60mV	-9.100mV	
112	165.8nA	44.20nA	12.00mV	3.800mV	-7.200mV	-2.700mV	
FINAL DATA							
FINAL TEMP (T_A)	300°C	300°C	300°C	300°C	300°C	300°C	
MIN VALUE	120.0nA	248.0nA	1.160V	914.0mV	877.0mV	766.0mV	
MAX VALUE	304.0nA	468.0nA	1.400V	976.0mV	999.0mV	786.0mV	
MEAN	185.3nA	323.8nA	1.264V	939.9mV	930.9mV	778.3mV	
STD DEV	52.44nA	56.17nA	82.77mV	16.40mV	42.50mV	5.651mV	

* NOTE: Catastrophic reject(s) removed from data after this point.



TABLE 7
FINAL DATA SUMMARY

PARAMETER	SPECIFICATIONS LIMIT		U N I T S	MEAN INT. DATA	AVERAGE Δ IN MEAN VALUE					
					POWER STRESS		TEMPERATURE STRESS I		TEMPERATURE STRESS II	
	MIN	MAX			SEM	MSC	SEM	MSC	SEM	MSC
I _R	-	1.0	μA		*+74.884	*+3.4183	*+2712.0	+45684	*+112.05	+10094
V _{F1}	.6	1.5	V		+0.05777	-0.00932	+0.00600	+0.00375	+0.01900	-0.00614
V _{F2}	.6	1.2	V		+0.01542	-0.00125	-0.30000	-0.00208	-0.01026	-0.00726

* NOTE: Catastrophic reject(s) removed from data after this point.



TABLE 8 STEP STRESS

CATASTROPHIC

FAILURE SUMMARY

JANTX1N5415

GROUP I POWER STRESS

TEST STEP	MFR A		MFR B	
	QTY.	NOTE	QTY.	NO. I/E
50% 50 hr.	0	-	0	-
100 hr.	5	A	0	-
100 hr.	2	A	0	-
250 hr.	0	-	0	-
100% 50 hr.	1	B	0	-
100 hr.	0	-	0	-
100 hr.	0	-	0	-
250 hr.	1	A	0	-
125% 10 hr.	0	-	0	-
15 hr.	0	-	0	-
25 hr.	0	-	0	-
100 hr.	0	-	0	-
100 hr.	2	B	0	-
250 hr.	JOB STOPPED		0	-
150% 10 hr.			0	-
15 hr.			0	-
25 hr.			0	-
100 hr.			0	-
100 hr.			0	-
250 hr.			3	B
175% 10 hr.			0	-
15 hr.			1	A
25 hr.			0	-
100 hr.			0	-
100 hr.			0	-
250 hr.	✓	✓	0	-

GROUP II 160 HR. TEMP. STEPS

TEST STEP (T _A)	MFR A		MFR B	
	QTY.	NOTE	QTY.	NOTE
75°C	8	A	0	-
100°C	JOB STOPPED		0	-
125°C			0	-
150°C			0	-
175°C			0	-
200°C			0	-
225°C			0	-
250°C			0	-
275°C			0	-
300°C			0	-

NOTES: A - I_R > 100μA

B - Visual failure - cathode lead detached due to stress

GROUP III 16 HR. TEMP. STEPS

TEST STEP (T _A)	MFR A		MFR B	
	QTY.	NOTE	QTY.	NOTE
150°C	6	A	0	-
175°C	1	A	0	-
200°C	0	-	0	-
225°C	0	-	0	-
250°C	0	-	0	-
275°C	0	-	0	-
300°C	0	-	0	-

MFR "A" - SEMTECH

MFR "B" - MICRO SEMICONDUCTOR



TABLE 9 STEP STRESS

PARAMETRIC

FAILURE SUMMARY

JANTX1N5415

GROUP I POWER STRESS

TEST STEP	MFR A		MFR B	
	QTY.	NOTE	QTY.	NOTE
50% 50 hr.	0	-	0	-
100 hr.	2	A	0	-
100 hr.	1	A	0	-
250 hr.	0	-	0	-
100% 50 hr.	1	B	0	-
100 hr.	0	-	0	-
100 hr.	1	A	0	-
250 hr.	0	-	0	-
125% 10 hr.	0	-	0	-
15 hr.	0	-	0	-
25 hr.	0	-	0	-
100 hr.	0	-	0	-
100 hr.	0	-	0	-
250 hr.	JOB STOPPED		0	-
150% 10 hr.			0	-
15 hr.			0	-
25 hr.			0	-
100 hr.			0	-
100 hr.			1	A
250 hr.			0	-
175% 10 hr.			0	-
15 hr.			0	-
25 hr.			0	-
100 hr.			0	-
100 hr.			0	-
250 hr.			0	-

GROUP II 160 HR. TEMP. STEPS

TEST STEP (T _A)	MFR A		MFR B	
	QTY.	NOTE	QTY.	NOTE
75°C	0	-	0	-
100°C	JOB STOPPED		0	-
125°C			0	-
150°C			0	-
175°C			0	-
200°C			0	-
225°C			0	-
250°C			0	-
275°C			5	A
300°C			6	A

GROUP III 16 HR. TEMP. STEPS

TEST STEP (T _A)	MFR A		MFR B	
	QTY.	NOTE	QTY.	NOTE
150°C	2	A	0	-
175°C	0	-	0	-
200°C	1	C	0	-
225°C	0	-	0	-
250°C	0	-	0	-
275°C	0	-	0	-
300°C	0	-	0	-

MFR "A" - SEMTECH

MFR "B" - MICRO SEMICONDUCTOR

NOTES: A - I_R limit failureB - V_{F1} maximum limit failure

C - S/N 7376 missing



APPENDIX A

FAILURE ANALYSIS

POWER STRESS



JANTX1N5415

FAILURE ANALYSIS

Date 1 December 1978

J/N 2CN242-14A P/N 1N5415 MFR SEMTECH

FAILURE VERIFICATION:Limit:
100 μ A Max.

S/N	PIV -volts-	I_R @ 50 V.dc	V_F @ _____dc	INITIAL REJ. AT TEST SEQUENCE NO.:	INITIAL REJ. FOR:
7363	380	< 0.1 μ A		11 (100% MRP 550 Hrs.)	Lead off
7366	330	< 0.1 μ A		27 (125% MRP 1250 Hrs.)	Lead off
7392	400 Uns, Inv	110 μ A		05 (50% MRP 150 Hrs.)	Lead off

VISUAL INSPECTION

All three Semtech samples have lost their external paint.

S/N 7363 and 7366 have a detached external lead (see Figure A-1).

S/N 7392 has cracked glass (see Figure A-2).

*^hFE trace present. Cannot meet stated test conditions. (Leaky)
**^hFE trace very leaky.

D=drift H=hysteresis Inv=inversion R=resistive S=soft Uns=unstable



JANTX1N5415

FAILURE ANALYSIS

Date 1 December 1978

J/N 2CN242-14A P/N 1N5415 MFR MICRO SEMICONDUCTOR

FAILURE VERIFICATION:Limit:
100 μ A Max.

S/N	PIV -volts-	I_F @ 50 V.dc	V_F @ ____dc	INITIAL REJ. AT TEST SEQUENCE NO.;	INITIAL REJ. FOR:
7419	80	< 0.1 μ A		41 (150% MRP 2025 Hrs.)	Lead off
7420	78	< 0.2 μ A		41 (150% MRP 2025 Hrs.)	Lead off
7421	98	< 0.1 μ A		41 (150% MRP 2025 Hrs.)	Lead off

INTERNAL VISUAL INSPECTION

All three Micro Semiconductor samples have lost their external paint and have a detached external lead (see Figure A-3).

*^hFE trace present. Cannot meet stated test conditions. (Leaky)
**^hFE trace very leaky.

D=drift H=hysteresis Inv=inversion R=resistive S=soft Uns=unstable



CONCLUSIONS

All of the samples except Semtech S/N 7392 were still within the electrical limits of the MSFC test when they became visual failures due to loss of an external lead. These structural failures were caused by exceeding the thermal design limits of the parts.

Semtech S/N 7392 exhibits instability and surface inversion due to moisture and other impurities which entered through the cracked glass.



ORIGINAL
OF FILE

JANTX1N5415

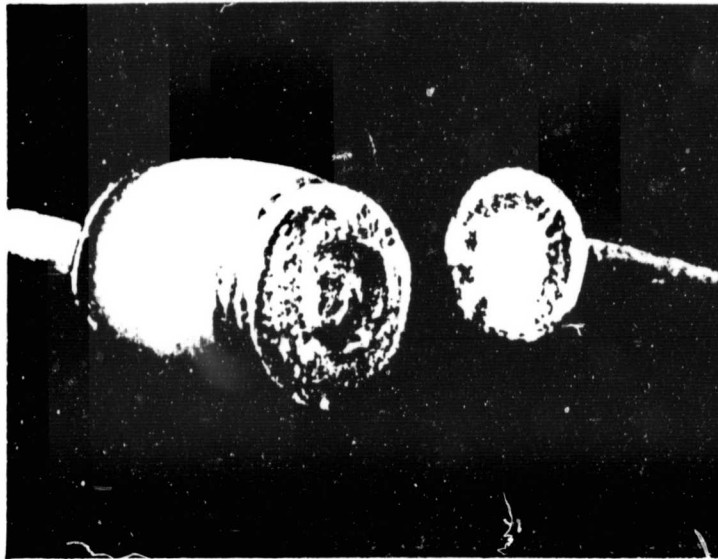


FIGURE A-1
S/N 7366. Typical Semtech Sample
With Detached Lead, 10X.

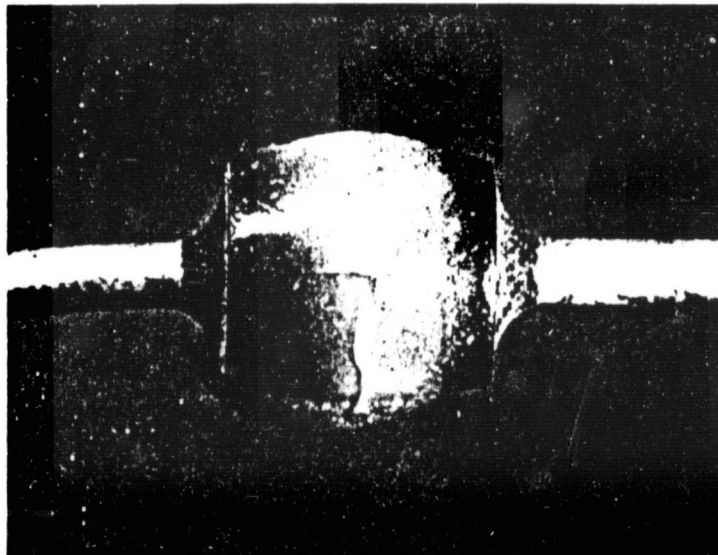


FIGURE A-2
S/N 7392, Semtech Sample
Showing Cracked Glass, 10X.



OR. C. 111
OF PGC 111

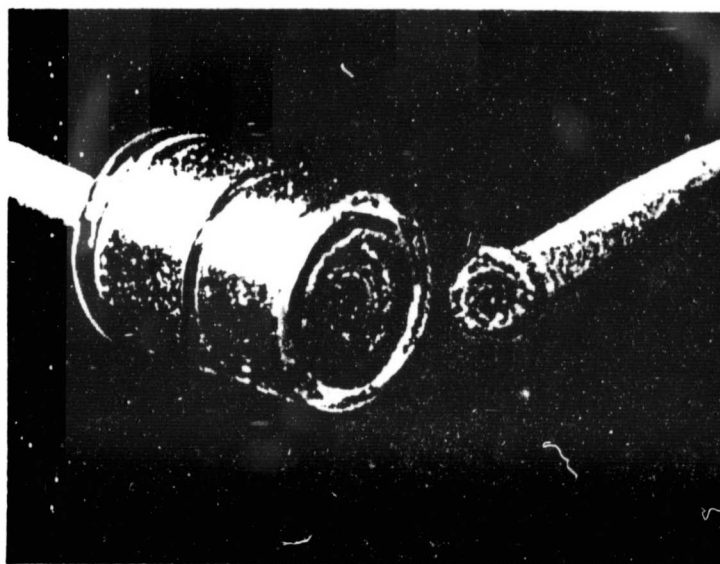


FIGURE A-3
S/N 7419. Typical Micro Semiconductor
Sample Displaying Detached Lead, 10X.



APPENDIX B

FAILURE ANALYSIS

TEMPERATURE STRESS



JANTX1N5415

FAILURE ANALYSIS

Date 1 December 1978

J/N 2CN242-14B P/N 1N5415 MFR SEMTECH

FAILURE VERIFICATION:Limit:
100 μ A Max.

S/N	PIV -volts-	I_R @ 50 V.dc	V_F @ _____ dc	INITIAL REJ. AT TEST SEQUENCE NO.;	INITIAL REJ. FOR:
7397	*R = 40K ** 425	>1mA <0.1 μ A		03 (75°C 160 Hrs.)	I_R
7399	*R = 50K ** 380	>1mA <0.1 μ A		03 (75°C 160 Hrs.)	I_R
7401	*R = 800K ** 375	>50 μ A <0.1 μ A		03 (75°C 160 Hrs.)	I_R

VISUAL INSPECTION

No visual anomalies were present.

CONCLUSION

These Semtech samples failed the reverse bias leakage test because of conductive external paint. When the continuity of the paint was interrupted by means of sandpaper, the reverse leakages fell to acceptable levels (see Figure B-1).

The glass on these samples was not hygroscopic as seen on previous Semtech samples.

* Resistive leakage is due to conductive external paint.

** These readings were taken after interrupting the paint conductive path.

*^hFE trace present. Cannot meet stated test conditions. (Leaky)
**^hFE trace very leaky.

D=drift H=hysteresis Inv=inversion R=resistive S=soft Uns=unstable



JANTX1N5415

ORIG
OF PL



FIGURE B-1
S/N 7397, Semtech Sample, 10X.
Interruption of paint conductive
path by abrasive paper.